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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,911	06/27/2003	Meng-Hsien Liu	405000	8149

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EXAMINER

DANG, KHANH

ART UNIT PAPER NUMBER

2111

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/607,911

Applicant(s)

LIU, MENG-HSIEN

Examiner

Khanh Dang

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 1, the phrase “a control unit for generating bus request and bus acknowledge signals of the two bus masters” is unclear and cannot be ascertained in view of the specification. In the originally filed specification, “[t]he at least one bus request signal is issued from the at least one integrated PCI interface card to the PCI host controller. The at least one bus acknowledge signal is issued from the PCI host controller to respond to the request of the at least one integrated PCI interface card. The at least one identification selection signal is issued from the PCI host controller for selecting and starting one of the bus masters in the integrated PCI interface card.” In addition, the essential structural cooperative relationships between the “at least two bus masters,” “a control unit,” and a “multiplexer” have been omitted, such omission amounting to a gap between the necessary structural connections. See MPEP 2172.01.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by the acknowledged prior art shown in Fig. 1.

As broadly drafted, these claims do not define any structure that differs from the acknowledged prior art of Fig. 1.

With regard to claim 1, the acknowledged prior art discloses an integrated PCI interface card (12), comprising: at least two bus masters (121 and 122); a control unit for generating bus request and bus acknowledge signals of the two bus masters; and a multiplexer for selecting an unused address to act as an identification selection signal of one of the at least two bus masters (at the outset, it is noted that the apparatus of the acknowledged prior art is a PCI apparatus and therefore, must be in full compliance with the PCI specification. Therefore, the PCI to PCI bridge 16, connected to the PCI host bridge via an upstream PCI bus and connected to the masters 121 and 122 via a downstream PCI bus, is readable as a control unit for generating bus request and bus acknowledge signals of the two bus masters. The most fundamental purpose of the PCI to PCI bridge is to increase the number of devices that a PCI system can support. In the instant case, the PCI to PCI bridge 16 provides support for the 2 masters 121 and 122. Further, accordance to the PCI specification, a bus request is issued from the integrated interface card 12 to the host controller 11, and the host controller issues an

acknowledged signal to the interface card 12 in response to the request. A typical PCI signal description, see PCI Local Bus Technical Summary, is shown below:

4.0 PCI Signal Descriptions

Required Pins -----		Optional Pins -----
<===AD[31:0]=====>	PCI Compliant Device	<===AD[63:32]=====>
<===C/BE[3:0]#====>		<===C/BE[7:4]#====>
<---PAR----->		<---PAR64----->
<---FRAME#----->		<---REQ64#----->
<---TRDY#----->		<---ACK64#----->
<---IRDY#----->		<---LOCK#----->
<---STOP#----->		
<---DEVSEL#----->		----INTA#----->
----IDSEL----->		----INTB#----->
<---PERR#----->		----INTC#----->
<---SERR#----->		----INTD#----->
<---REQ#----->		<---SBO#----->
----GNT#----->		<---SDONE----->
----CLK----->		<---TDI----->
----RST#----->		----TDO----->
		<---TCK----->
		<---TMS----->
		<---TRST#----->

Since the PCI bus is a multiplexed bus, an address signal precedes data on the same bit lines. Therefore, a 32-bit data bus will necessarily provide a 32-bit address signal as well. If the bus is a 64-bit line bus, then the extension contains mainly another 32 multiplexed address and data lines, plus extra power and ground rails. See How the PCI Bus Works. Since the downstream bus, connected to the PCI-PCI bridge, is also a PCI bus, it is clear that the address bits of the two masters 121 and 122 must be multiplexed in accordance to the PCI specification. It is also clear that unused address

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bits in the PCI address space must be used for identify a corresponding bus master and for selecting the bus master in accordance to the PCI specification. Note that it is inherent to use a multiplexer for performing an act of multiplexing.

With regard to claim 2, it is clear that since the masters 121 and 122 share the same interface provided by the card 12 and the same slot provided by the PCI bus, they must share the same interrupt signal.

With regard to claim 4, it is clear that Fig. 1 shows a PCI bus system having host controller 21. Note that in accordance to the PCI specification, the host controller includes an arbiter for bus arbitration for interface cards, the IDSEL is issued by the PCI host controller for selecting one bus master of the integrated PCI interface card (see IDSEL of the signal description shown above).

With regard to claim 5, it is clear that Fig. 1 further comprises additional PCI card (23, for example) comprising a bus master (231, for example).

With regard to claim 6, it is clear that since the masters 121 and 122 share the same interface provided by the card 12 and the same slot provided by the PCI bus, they must share the same interrupt signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art of Fig. 1.

As discussed above, the acknowledged prior art of Fig. 1 discloses the claimed invention including the use of arbitration for granting access to the PCI bus. As a matter of fact, every PCI system must includes arbitration (see at least How PCI Works). The acknowledged prior art does not specifically disclose the use of arbitration based on rotating or round robin. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use round robin or rotating arbitration, since the use of round robin arbitration in PCI system is old and well-known as evidence from Altera, PCI Bus Arbiter, cited below. The Altera PCI Bus Arbiter implements either rotating priority or a fixed priority scheme. In the rotating priority scheme, the requestor that is most recently granted the bus receives the lowest priority, while the requestor position next to it receives the highest priority. The remaining requestor receives subsequently lower priority based on its position. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use rotating arbitration in the PCI bus system of Fig. 1, since the Examiner takes Official Notice that the use of such rotating arbitration is old and well-known; and using round robin or rotating scheme in the arbitration system of Fig. 1 only involves ordinary skill in the art.

Allowable Subject Matter

Claims 3 and 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

U.S. Patent Nos. 5,594,882 to Bell, 5,944,805 to Ricks et al., 6,408,347 to Smith et al., 5,832,238 to Helms, Tech-Pro (How the PCI Bus Works), Altera PCI Bus Arbiter, and PCI Local Bus Technical Summary are cited as relevant art. In particular, Bell discloses a bus architecture utilizing multiplexed address and data signals on a bus wherein, the unused address provided by the extension provided by the 64 bit PCI bus is used for identifying the originated master. According to Bell, since the other 16 bits of a 64-bit address signal are not utilized in a PCI bus standard, these upper unused address bits are utilized for identifying the originated master.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.



Khanh Dang
Primary Examiner